REMARKS

In response to the Office Action mailed May 5, 2004, Applicants respectfully request reconsideration. To further the prosecution of this Application, Applicants submit the following remarks, have canceled claims and have added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-22 were pending in this Application. By this Amendment, claims 7, 15 and 19 have been canceled. Additionally, claims 23-28 have been added. Accordingly, claims 1-6, 8-14, 16-18 and 20-28 are now pending in this Application. Claims 1, 12, 18 and 22 are independent claims.

Rejections under §102 and §103

Claims 1-6, 8-9, 11-14, 16-18 and 20-22 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,708,771 (Brant et al.). Claims 7, 10, 15 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Brant et al.

Applicants respectfully traverse the rejection of claims 7 and 15, and request reconsideration. To further the prosecution of this Application, Applicants have (i) amended independent claim 1 to include all of the limitations of claim 7 which originally depended from claim 1 and (ii) canceled claim 7. Similarly, Applicants have (i) amended independent claim 12 to include all of the limitations of claim 15 which originally depended from claim 12 and (ii) canceled claim 15. Furthermore, Applicants have made an amendment to independent claims 18 and 22 so that independent claims 18 and 22 include limitations similar to those recited in claim 15, and canceled claim 19. Applicants respectfully submit that the claims are now in allowable condition as will now be explained.

Brant et al. discloses a data processing system having a variety of components (column 5, lines 3-12). The system includes a power distribution arrangement in which cached disk array controllers 60 and 70 are energized by power supplies 46 and 50 (column 6, lines 61-65, and Fig. 4). The relationship

between these power supplies and the elements of one of the controllers 60 is presented in Fig. 3 (column 6, lines 65-67). That is, Fig. 3 is a system block diagram of disk array controller 60 illustrating its relationship to the redundant power system arrangement in accordance with the Brant system (column 6, line 67 through column 7, line 3).

With further reference to Brant, the power supplied to the controllers 60 and 70 is segregated such that failure of either power supply 46 or 50 will not cause data loss in both of the memories of either controller (column 7, lines 4-7). This is important where those memories are used in a mirrored configuration to hold write data received from the host (column 7, lines 7-9). If either power supply 46 or 50 fails so that primary power is lost to one of controllers 60 or 70, the other controller employs a serial dump link 22A to recover the host write data contained in the fast memory associated with the first controller which data is then written to one or more disks (column 7, lines 9-14).

As seen in Figs. 3 and 4 of Brant, power supply 46 provides main power over power bus 48 which is connected for energizing all of the components of controller 60 Column 7, lines 15-17). Connection 61 from main power bus 48 likewise provides power via a coupler formed from diodes 62 and 63 into power bus 64, and hence into a subset of certain selected key elements of controller 60 (column 7, lines 17-21). As shown, these elements include crystal oscillator 55, memory controllers 12A and 12B, and DRAM 20 (column 7, lines 21-23). This power distribution is illustrated in Fig. 3 wherein the stippled or gray shaded components are power by main power bus 48 alone, while the clear elements are powered by both bus 48, as well as by the auxiliary power source 51 from power supply 50 (column 7, lines 23-27).

With further reference to Brant, auxiliary power output 47 of power supply 46 is similarly connected to the other controller 70 where it is OR coupled via diodes 72 and 73 into secondary power bus 74 to drive a subset 75 of components which correspond to the components driven by secondary power bus 64 in controller 60 (column 7, lines 28-33). Main power bus 52 of power

supply 50 is coupled to energize all components of controller 70 including connection 71 which is diode OR coupled so as to enable components 75 (column 7, lines 33-36).

Again, with further reference to Brant, failure of a power supply 46 or 50, as by shorting of a bypass capacitor for example, could short the power bus on a controller (column 9, lines 6-8). However, the primary and secondary memory controllers remain powered through the connection to the auxiliary power output for the other controller power source (column 9, lines 8-11). Fig. 3 shows that loss of power source 46 will cause all the shaded components to cease operation (the disk drives themselves are supplied by yet other power sources) while primary controller 12A and the secondary controller 12B, along with memory 20, remain active (column 9, lines 11-15).

Claims 1-11

As mentioned above, Applicants have amended independent claim 1 to include all of the limitations of claim 7 which originally depended from claim 1 and then canceled claim 7. Claim 1, as amended, is directed to an electronic system including critical circuitry, non-critical circuitry having a first section and a second section, and a power sub-system. The power sub-system has a first power assembly, a second power assembly, and a set of connections which is configured to connect the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry. X and Y are integers greater than 0. The first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the

first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail. The second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

As the basis of the rejection of claim 7 (which is now claim 1 in independent form), the Office Action contends that Brant discloses removal of faulted power supplies and that the concept of defining a device as failed when a portion of the device has failed is well known (see page 9, last paragraph of the Office Action). The Office Action then contends that it would have be obvious to cease providing power to a device when a portion of the power system has failed, thus increasing the chance that a failure will now propagate through the power system once detected and thus creating a more predictable system which is often sought in critical systems (see page 9 last paragraph through page 10 first paragraph of the Office Action).

Applicants respectfully disagree with the Office Action's analysis and submit that such analysis is misplaced. Whether Brant discloses removal of faulted power supplies and whether the concept of defining a device as failed when a portion of the device has failed is well known is irrelevant. In order to establish a *prima facie* case of obviousness, the Office Action must meet three criteria.

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or

references when combined) must teach or suggest all the claim limitations."[1]

Brant does not teach or suggest all of the claim limitations of claim 1 as amended. For example, Brant does not teach or suggest an electronic system including a power sub-system which has a first power assembly including multiple first power supplies that perform a normal operating procedure to provide power to critical circuitry and to a first section of non-critical circuitry when up to X first power supplies fail and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail, as recited in claim 1. Rather, as mentioned above, the Brant power supplies 46 and 50 are illustrated simply as general boxes. Applicants cannot find any mention of either the Brant power supply 46 including multiple power supplies, or the Brant power supply 50 including multiple power supplies. Since this is so, Brant cannot teach or suggest multiple first power supplies that perform a normal operating procedure to provide power to critical circuitry and to a first section of non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail, as recited in claim 1. Furthermore, Brant cannot further teach or suggest multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to a second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the second section of the non-critical circuitry when more than Y second power supplies fail, as recited in claim 1.

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[1] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Since there is no teaching or suggestion of these limitations in Brant, claim 1 patentably distinguishes over the cited prior art. Accordingly, claim 1 is now in allowable condition and the rejection of claim 1 should be withdrawn.

If the rejection of claim 1 is to be maintained, Applicants respectfully request that it be pointed out with particularity where each limitation is taught or suggested by Brant.

Because claim 2-6 and 8-11 depend from and further limit claim 1, claims 2-6 and 8-11 are in allowable condition for at least the same reasons. Applicants further wish to point out that the dependent claims recite additional novel limitations and thus further patentably distinguish over the cited prior art as well.

For example, in connection with claim 2, suppose that one were to argue that Brant's power supply 46 is the first power assembly of the power sub-system recited in claim 2 and that Brant's power supply 50 is the second power assembly of the power sub-system recited in claim 2. The Office Action's contention in the middle paragraph of page 3 that Brant is incorrect. Brant does not disclose a first section of non-critical circuitry including a first set of storage devices, and a second section of the non-critical circuitry including a second set of storage devices powered by the power sub-system, as recited in claim 2. Rather, Brant discloses disk drives which are supplied by power sources other than power sources 46 and 50 (see column 9, lines 11-15 of Brant). Accordingly, claim 2 further patentably distinguishes over the cited prior art.

As another example, in connection with claim 3, Brant does not disclose that the second set of storage devices is configured to mirror data on the first set of storage devices. That is, the Office Action's contention that Brant discloses a second set of storage devices to mirror data on a first set of storage devices is incorrect (see the first paragraph on page 4 of the Office Action). Brant does mention fast mirrored memory (e.g., see Fig. 2 of Brant). However, Applicants cannot find any mention of mirroring by sets of storage devices in Brant. Accordingly, claim 3 further patentably distinguishes over the cited prior art.

Claims 12-17

As mentioned earlier, Applicants have amended independent claim 12 to include all of the limitations of claim 15 which originally depended from claim 12 and canceled claim 15. Claim 12, as amended, is directed to a power system for providing power to electronics including critical circuitry and non-critical circuitry. The power system includes a first power assembly, a second power assembly, and a set of connections which is configured to connect the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry. X and Y are integers greater than 0. The first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail. The second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

As mentioned above in connection with claim 1, the cited prior art does not teach or suggest such a power sub-system. Accordingly, claim 12 patentably distinguishes over the cited prior art for at least the same reasons as claim 1.

Thus, claim 12 is in allowable condition and the rejection of claim 12 should be withdrawn.

Because claim 13-17 depend from and further limit claim 12, claims 13-17 are in allowable condition for at least the same reasons.

Claims 18-21

As mentioned earlier, Applicants have made an amendment to independent claim 18 so that it includes limitations similar to those recited in claim 15, and then canceled claim 19. Claim 19, as amended, is directed to a method for providing power to electronics including critical circuitry and non-critical circuitry. The method includes the step of operating a first power assembly to power the critical circuitry and a first section of the non-critical circuitry. The first power assembly is equipped with A+X power supplies and being configured to continue to operation when up to X power supplies of the A+X power supplies individual fail. The method further includes the step of operating a second power assembly to power the critical circuitry and a second section of the non-critical circuitry. The second power assembly is equipped with B+Y power supplies and being configured to continue to operation when up to Y power supplies of the B+Y power supplies individual fail. The method further includes the steps of, in response to a failure of more than Y power supplies of the second power assembly, continuing to power the critical circuitry and the first section of the non-critical circuitry using the first power assembly; and in response to a failure of more than X power supplies of the first power assembly, continuing to power the critical circuitry and the second section of the non-critical circuitry using the second power assembly.

As mentioned above in connection with claim 1, the cited prior art does not teach or suggest such operating a first power assembly having A+X power supplies, and a second power assembly having B+Y power supplies, as recited in claim 18. Accordingly, claim 18 patentably distinguishes over the cited prior

art for at least the same reasons as claim 1. Therefore, claim 18 is in allowable condition and the rejection of claim 18 should be withdrawn.

Because claim 19-21 depend from and further limit claim 18, claims 19-21 are in allowable condition for at least the same reasons.

Claim 22

Claim 22 is directed to an electronic system having critical circuitry, non-critical circuitry having a first section and a second section, and a power sub-system. The power sub-system includes a first power assembly, and a second power assembly. The power sub-system further includes means for connecting the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry. X and Y are integers greater than 0. The first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail. The second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

As mentioned above in connection with claim 1, the cited prior art does not teach or suggest such an electronic system. Accordingly, claim 22 patentably distinguishes over the cited prior art for at least the same reasons as claim 1. As a result, claim 22 is in allowable condition and the rejection of claim 22 should be withdrawn.

Newly Added Claims

Claims 23-28 have been added and are believed to be in allowable condition. Claims 23-25 depend from claim 1. Claims 26-28 depend from claim 12. Support for claims 23-28 is provided within the Specification, for example, on page 10 , line 14 through page 12, line 18; page 13, lines 26 through page 15, line 3; and Figs. 2 and 4. No new matter has been added.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicants' Representative at the number below.

Applicants hereby petition for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,

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